LaPlace Transforms in Design and Analysis of Circuits

Part 5: Active Circuit Design & Analysis

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Credit: 5 PDH

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Part 5
by Tom Bertenshaw

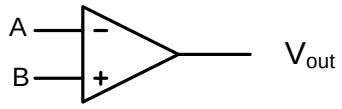
Active Circuit Design and Analysis

A Generic Device

For the present we will restrict active circuits to be designed around a class of amplifiers and filters implemented using Operational Amplifiers (OpAmps) for two reasons: a) they possess a very high input impedance (an FET input), and b) their input circuitry contains a differential amplifier that, when coupled with external feedback, drives the difference between its two inputs to be zero. There are certainly other attributes to OpAmps, but for now we will use just these two in developing an ensemble of basic building block circuits. We will assume the gain-bandwidth product, source and sink currents, slew rate, etc. of the OpAmp are sufficient for our purposes. In other words, we are leaving the study of OpAmps themselves to another course.

Further, since the necessary DC power circuitry seldom impacts the response of active amplifiers and filters beyond setting upper and lower bounds on voltage excursions, we will also forgo those considerations in this module. Suffice it to say that we will work with a generic device limited to excursions of $\pm 15V$. If other values are necessary at any point, they will be identified.

At this juncture, just keep in mind the salient feature of very high input impedance[1]; so high that when compared to external circuitry current flow values, any current flow into the OpAmp can be ignored (nano amps). This is another of those For-All-Practical-Purposes events). Also, keep in mind that external feedback causes the difference in input values to be driven to zero (there will always be external feedback as the open loop gain of an OpAmp is at, or over, a factor of 10^5). So, the characteristics to keep in mind are a) no input current; and b) input A is driven to be the same voltage potential as input B.

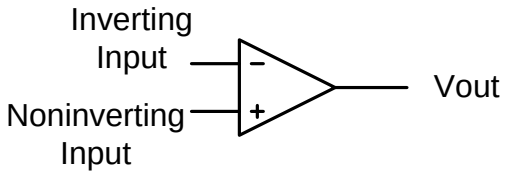


The OpAmp is basically a voltage driven voltage device, and gains are usually taken to mean voltage gain. The OpAmp will sink and source current to the external circuitry however, and the manufacturer's data sheet for the particular device under consideration will detail those and all other relevant parameters necessary to successfully use the device.

[1] a few megohms, or less, for PN junction devices to tens or even hundreds of megohms for FET's

Our generic OpAmp looks like (schematically):

Circuit #1

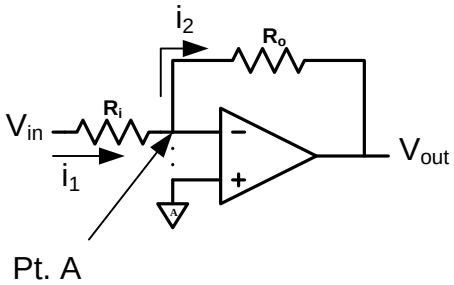


When a positive going signal is applied to the inverting input it appears at the output as a negative going signal, i.e., it is inverted. When a positive going signal is applied to the non-inverting input, it appears at the output as positive going signal, i.e., its polarity is preserved. Because of transit times there will be a small phase shift in the output, but that effect is also assumed to be trivial for our purposes.

Basic Amplifiers

Inverting Amplifier

Circuit #2



Point A is at the same potential as the non-inverting input; it is a virtual ground at zero volts potential (in **actual** design practice there is a small output offset caused by a trivial input current, but FAPP (For All Practical Purposes[2]) the potential is caused to be zero through a DC offset input (not shown) on the OpAmp).

Since no current flows into the OpAmp, $i_1 = i_2$, using that fact:

$$\frac{V_{in} - 0}{R_i} = \frac{0 - V_{out}}{R_o}$$

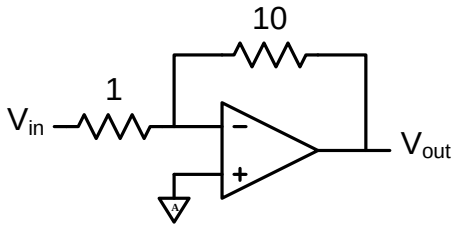
Re-arranging:

[2] John S. Bell, 1928-1990, Physicist Extraordinaire

$$\frac{V_{out}}{V_{in}} = -\frac{R_o}{R_i}$$

Since $-\frac{R_o}{R_i} = \frac{R_o}{R_i}\angle 180$, the minus sign simply means that there is a **phase inversion**.

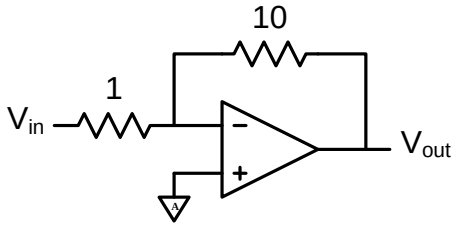
For example:



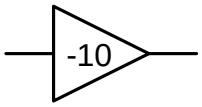
Assume $V_{in} = \sin(5t)$, then the transform is:

$$V_{out} = -10\sin(5t) \text{ or } V_{out}(s) = \frac{-50}{s^2 + 25}$$

For convenience:



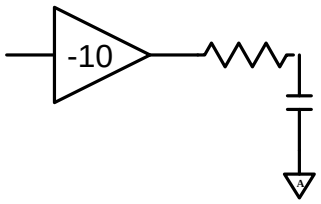
may be represented by the shorthand schematic:



The second symbol is understood to be identical to the first as far as circuit behavior in all parameters is concerned. It is merely shorthand. Bear in mind that the first, or upper, schematic symbol is also a shorthand version of the detailed engineering drawing used for production. Those details will not be addressed in this series of modules, but are reserved for a course dealing in OpAmp fundamentals.

An example of use:

Low Pass Circuit



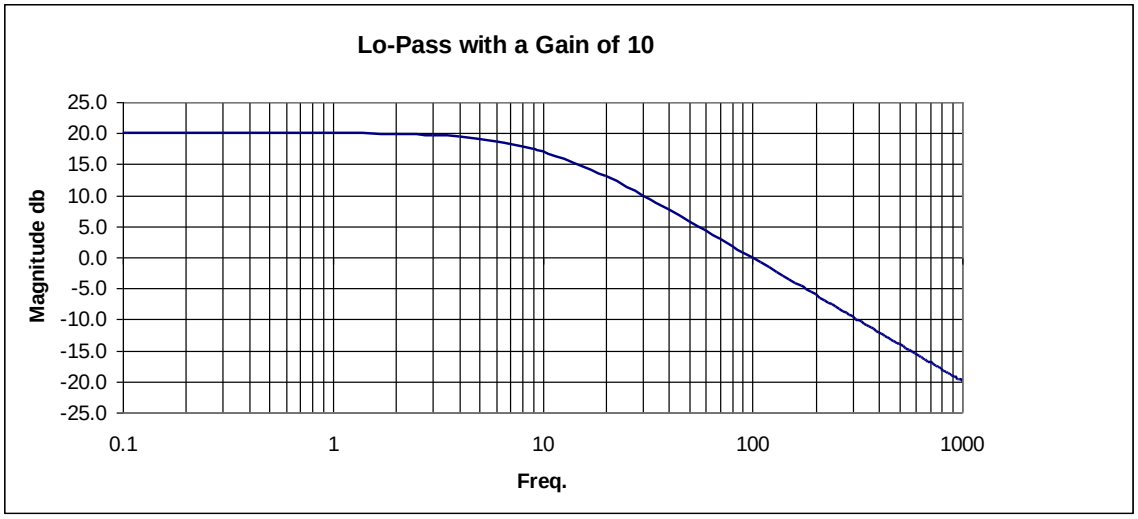
For the above circuit, assume RC=.1, and bear in mind that the minus sign represents a 180^o phase change at the output, but the absolute value of the amplification is 10. Then, the transfer function is:

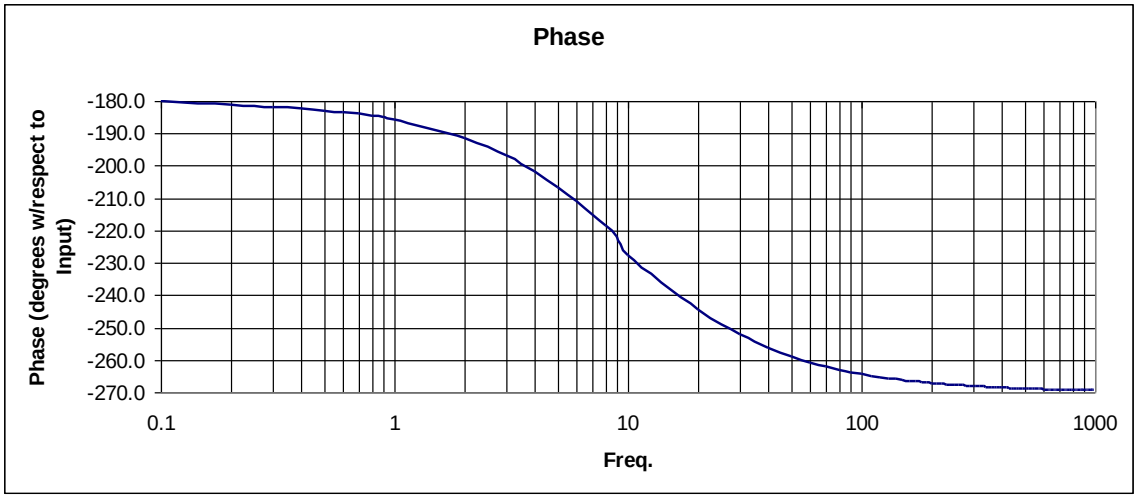
$$\frac{V_{out}}{V_{in}} = \frac{100 \angle 180}{s + 10}$$

and the plotting equations are:

$$Mag\ . = 20 \log(10) - 20 \log\left(\sqrt{1 + \frac{\omega^2}{100}}\right)$$

$$Phase\ = -180\ - \tan^{-1}\left(\frac{\omega}{10}\right)$$





Let's extend this exercise to include a driver of sin(100t). Than the transfer function is:

$$V_{out}(s) = \frac{-10000}{(s+10)(s^2+10^4)} = \frac{.9\angle -180}{s+10} + \frac{(.995)(100)\angle 95.7^o}{s^2+100^2}$$

Because it was known that the output phase with respect to the input varied between -180 and -270 (+90) minus what was chosen as the operator on the angle. Be careful when using arctan in your calculator or software program; some devices only return answers for quadrants I & IV and its left to you to keep track of the quadrant you are in. Question: Why in the above example is the output magnitude less than 10?

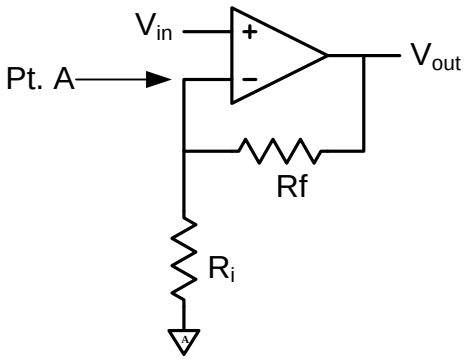
The Bode plot predicts an output of 1*input @ -265^o for an input at 100 rads/s. That prediction closely approximates the calculated result. There is a small amount of error in the calculations for both the plots and the calculated result due to round off (which is an arbitrary choice).

Completing the analysis for the above circuit, using a FAPP approach:

$$V_{out}(t) \approx \sin(100\,t - 264^o) - .9e^{-10\,t}$$

Non-inverting Amplifier

The non-inverting amplifier schematic (non-detailed) looks like:



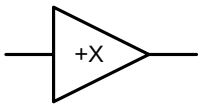
The voltage at point A is:

$$V_{Pt.A} = \left(\frac{R_i}{R_i + R_f} \right) V_{out}$$

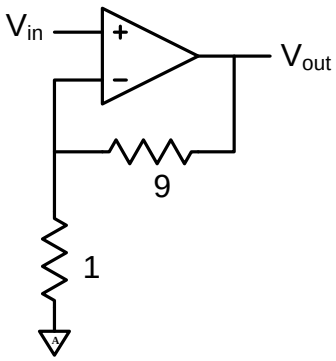
But the voltage at point A must also equal V_{in} because of the external feedback network of R_i & R_f, so re-arranging:

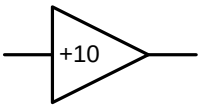
$$\frac{V_{out}}{V_{in}} = 1 + \frac{R_f}{R_i}$$

Its shorthand version is:



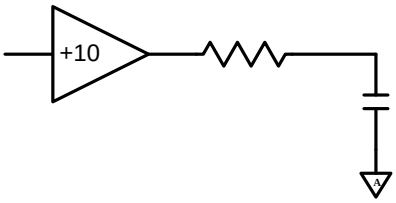
where X is the numerical value of the gain. So, an amplifier with a gain of 10 would look like:





A note of caution is warranted here. In these modules values are chosen to illustrate a point. In practice resistances of 1Ω & 9Ω may not be practical because of current draw and I^2R heating in the OpAmp; but it should be clear that R_f must be 9X the value of R_i to achieve a gain of +10. Choose R_i and R_f with a view to limiting the current draw from the OpAmp; 100 & 900 ohms would limit the current draw to 15ma when the supply is $\pm 15V$.

Repeating the exercise for the inverting OpAmp, but as a non-inverting amplifier with RC=.1:



The transfer function is:

$$\frac{V_{out}}{V_{in}} = \frac{100}{s+10}$$

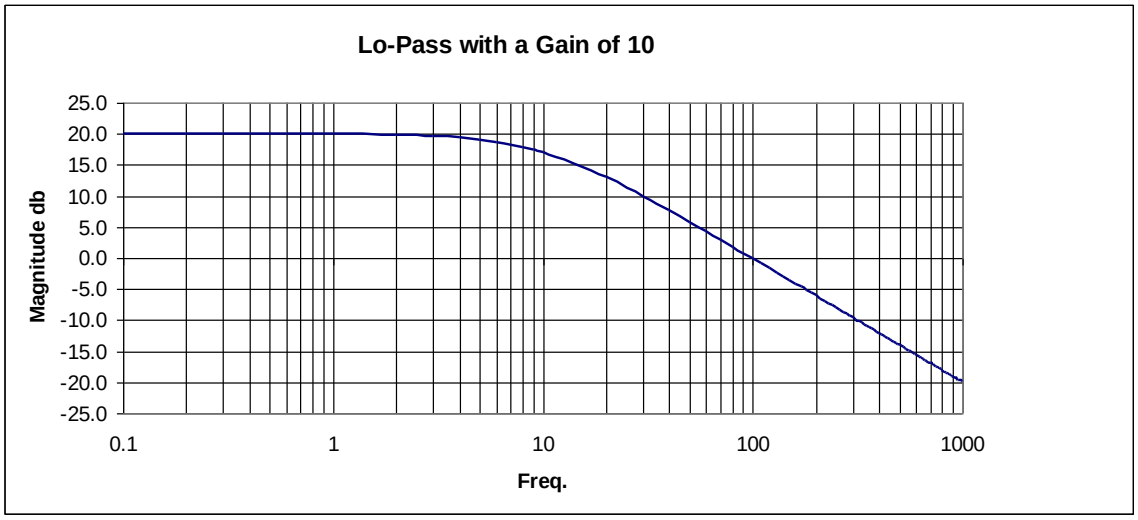
The plotting equations unsurprisingly are:

$$Magnitude \quad = 20\log(10) - 20\log\left(\sqrt{1+\left(\frac{\omega}{10}\right)^2}\right)$$

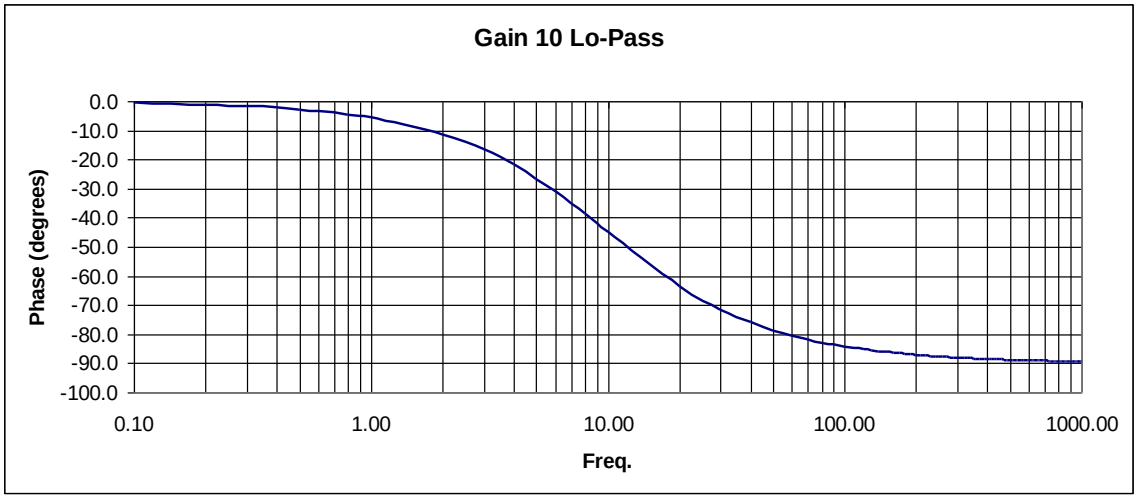
and

$$Phase = 0 - \tan^{-1}\left(\frac{\omega}{10}\right)$$

The magnitude plot is identical to the plot for the -10 voltage gain lo-pass.



But the phase plot has different values on the Y axis.



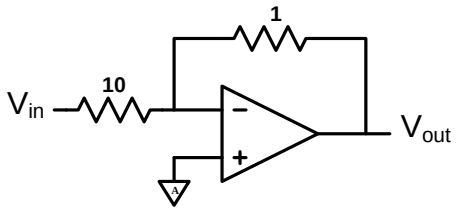
This time, we will drive the system with sin(10t). The transfer function is now:

$$V_{out} = \frac{1000}{(s+10)(s^2+10^2)} \approx \frac{.1}{(s+10)} + \frac{(7.07)(10)\angle -45^o}{\left(s^2+10^2\right)}$$

The steady state amplitude of 7.07 is nicely consistent as the -3db point is .707 of max. Since max is 10 in this case, our answer checks.

The net result of combining a voltage gain amplifier with a lo-pass filter is merely to change the operating amplitude from a 0db floor. Of course an attenuator will also function in a similar fashion. Notice that in the impulse response transfer function the amplifier affects the magnitude of N(s) and does nothing to D(s). Ideally that is what we are after; but in practice the OpAmp will not be ignored and it will impress its gain-bandwidth product (GBW) on the output. We generally ignore that troublesome fact in pedagogic treatises as the assumption is that the GBW is many times the bandwidth needed. Sadly, in real life as we deal with frequencies tending into the microwave region, consideration of the actual operating parameters of the OpAmp cannot be ignored, and models such as S parameters become convenient. But, that tale is left for another time. For now assume the GBW of the OpAmp is sufficient to pass undiminished any signal within the bandwidth of our pedagogic interest.

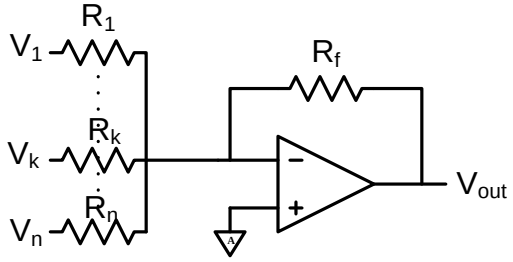
An attenuator with a gain of $|.1|$ looks like:



This attenuator is preferred over a simple voltage divider as any circuitry to the right of V_{out} is invisible to the driver (V_{in}). These are great devices for isolating one circuit from another and bypassing the loading problem.

The Summer

The summer is a utility workhorse circuit. Its function is to sum N inputs into a single output. Simultaneously with summing, this circuit can be used to apply tailored gains to each of its N inputs. Its schematic looks like:



There are some rules to be observed when using a summer; it is required to operate in its linear region of amplification so that superposition applies. Non-linear operation of any input destroys information as the output is forced to a voltage rail (i.e., DC power supply

voltage); voltage rail outputs can not distinguish between input variations, i.e., input information is lost as the sum of input excursions causes a collision with the rail. Secondly, the input to the inverting input must be a virtual ground; this is accomplished by causing the non-inverting input to be at 0 volts potential (you will know that it is adjusted correctly if all inputs are grounded and $V_{out} = 0$).

Beginning the analysis:

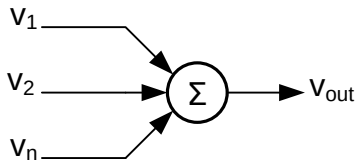
$$V_{out}(V_1) = -\frac{R_1}{R_f}V_1$$
$$\vdots$$
$$\vdots$$
$$V_{out}(V_k) = -\frac{R_k}{R_f}V_k$$
$$\vdots$$
$$\vdots$$
$$\vdots$$
$$V_{out}(V_n) = -\frac{R_n}{R_f}V_n$$

Summing them all:

$$V_{out} = -\left(\frac{R_1}{R_f}V_1 + \text{.....} \ . + \frac{R_k}{R_f}V_k + \text{.....} \ \text{....} + \frac{R_n}{R_f}V_n\right)$$

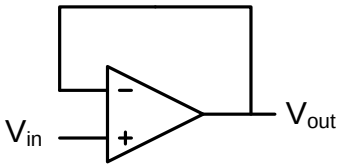
Bear in mind that it is prudent to require V_{out} to maintain a small potential below the positive rail and a small amount above the negative rail as a margin of safety; usually 1v is sufficient.

The shorthand symbol for a summer is:



The Buffer

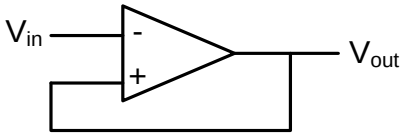
We have one more elementary circuit to consider before we begin the discussion of the more complex basic circuits; and that elementary circuit is the buffer. Its schematic is:



The transfer function is:

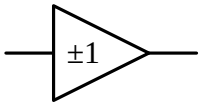
$$V_{in} - V_{out} = 0 \text{ or re-arranging } V_{out} = V_{in}$$

And for this one:

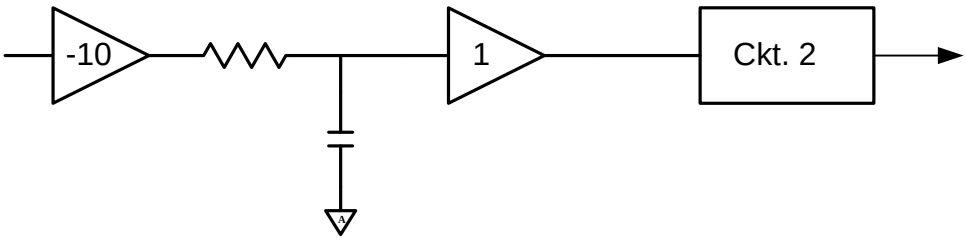


$$V_{in} + V_{out} = 0 \text{ or } V_{out} = -V_{in}$$

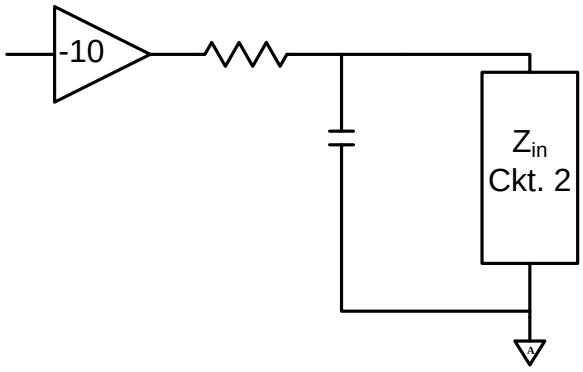
The utility of this circuit is two fold; a) it has a sufficiently high input impedance that it does not load the circuit providing V_{in} and b) its output impedance is very low to the circuit that the buffer is providing V_{out} to; i.e., it looks like an ordinary low impedance voltage supply. It provides major design advantages in that it isolates one circuit stage from another, minimizing loading effects and maximizing voltage transfer from stage to stage. Its shorthand schematic is:



An illustration of use:



The buffer prevents input impedance of Ckt. 2 from appearing in parallel with the lo-pass filter. This arrangement preserves the filter's transfer function by not allowing the input impedance of Ckt. 2 to alter the impedance and/or voltage division ratio of the filter. For example, if the buffer were not there, then the filter impedance is altered in this way:



The lo-pass transfer function with the buffer is:

$$\frac{V_{out}}{V_{in}} = \frac{-10\left(\frac{1}{RC}\right)}{s + \frac{1}{RC}}$$

Without the buffer the transfer function becomes:

$$\frac{V_{out}}{V_{in}} = \frac{-10\left(\frac{1}{RC}\right)}{s + \frac{1}{Z_{in}C} + \frac{1}{RC}}$$

Clearly the break frequency has shifted and the shift is dependent on Z_{in}. But if Z_{in} is complex, then in turn, it is a function of frequency; this is a nasty loading problem. Use a buffer to obviate that un-necessary complication. **Task:** Derive the above equation by considering that the current through the resistor must equal the current through the parallel combination of Z_{in} & $1/sC$.

One last point: with the buffer in the circuit, the parallel combination of Z_{in} (of the buffer) and the capacitor is:

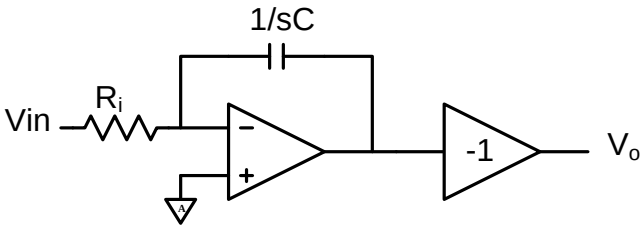
$$Z_p = \frac{Z_{in} X_C}{Z_{in} + X_C}$$

Because $Z_{in} >> X_c$, $Z_p \rightarrow X_C$ and the loading problem vanishes towards zero. Older engineers can recognize the similes between the solid state buffer and a vacuum tube triode amp with unity gain.

Mathematical Function Circuits

The Integrator

Consider the following circuit:



The transfer function is:

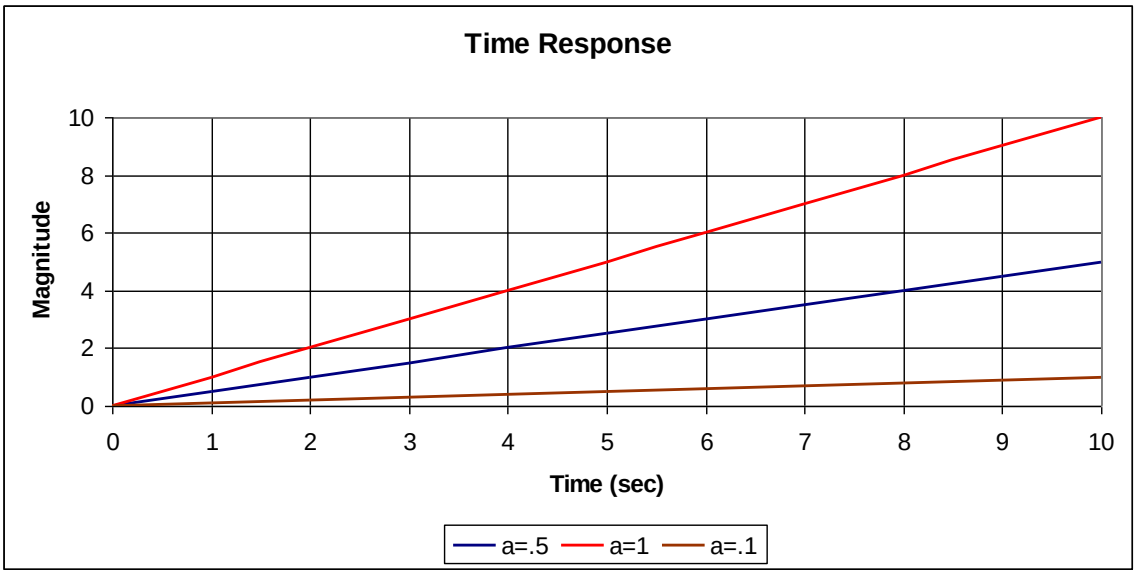
$$\frac{V_o}{V_{in}} = \frac{1}{sRC} = \frac{\alpha}{s}$$

when V_{in} is a unit step, then:

$$V_o = \frac{\alpha}{s^2}$$

The time response, as a function of α is:

$$V_o(t) = \alpha t$$



This circuit presents a linear voltage rise as a function of time; as such, it has utility as a timer that uses voltage comparisons as a trigger, or in any circuit that requires a linear rise with respect to time. As a designer, you have control over the slope via choosing the combination of RC that suits your purpose.

So, when the input is a unit step, this circuit integrates. But what if the input is a sinusoid? In that case:

$$V_0 = \frac{a\,\omega_o}{s\left(s^2 + \omega_o{}^2\right)} = \frac{\frac{\alpha}{\omega_o}}{s} + \frac{\frac{\alpha}{\omega_o}\angle -90}{s^2 + \omega_o^2}$$

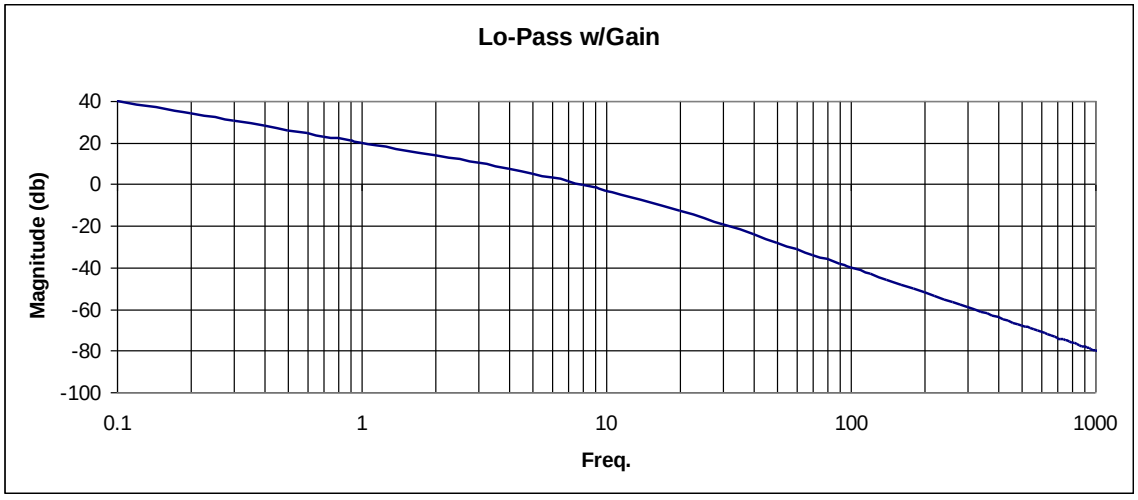
$$V_o(t) = \frac{\alpha}{\omega_o}\left(u(t) + \sin(\,\omega_o t - 90^{\,o})\right)$$

which is essentially a sinusoid riding a DC potential of $\frac{\alpha}{\omega_o}$. For the sake of illustration, assume the usual RC=.1, and that $\omega_o = 10$.

The plotting equation:

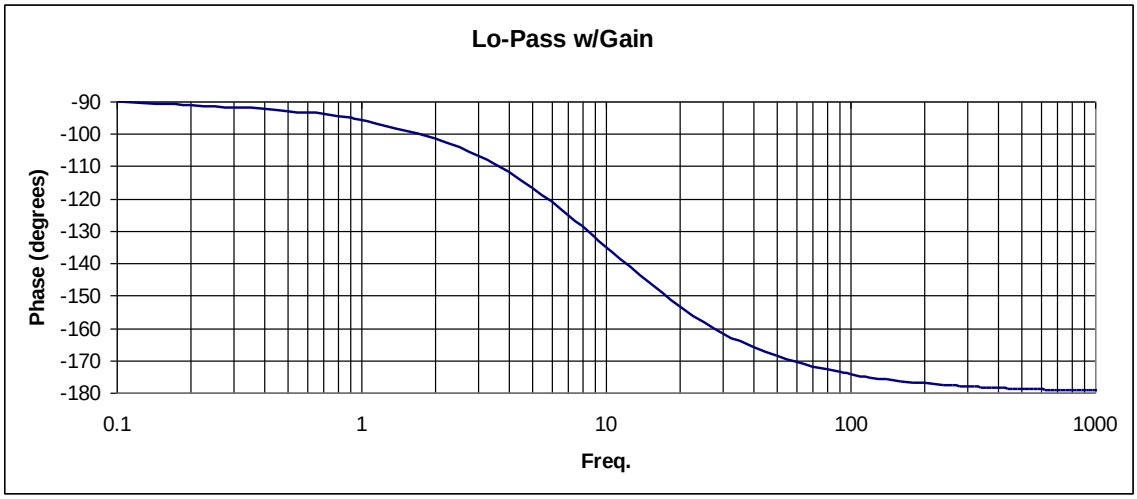
$$Magnitude \;\; = 20\log(100) - 20\log(\omega) - 20\log\left(\sqrt{1 + \left(\frac{\omega}{10}\right)^2}\right)$$

The Integrator has now become a Lo-Pass filter with a controlled gain.



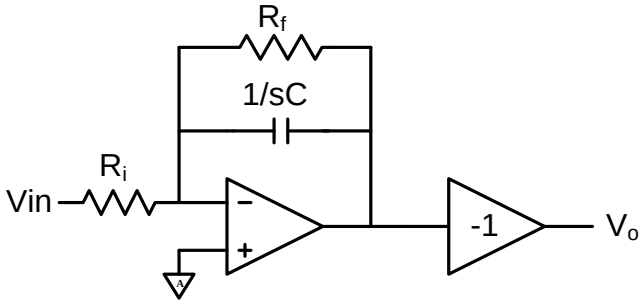
As expected, there is -20db/decade roll-off until 10 rads/s. At that point the roll-off increases to -40 dc/dec. Since we have established that with a step input this circuit

integrates, we should expect a gain in very low frequencies, and indeed there is a significant gain.



Changing the Break Point: **Integrator/Lo-Pass with Gain**

Consider this circuit:



Step one is to develop a suitable expression for the parallel combination of $\frac{1}{sC}$ & R_f.

$$\frac{\frac{R_f}{sC}}{R_f + \frac{1}{sC}} = \frac{R_f}{sCR_f + 1} = \frac{\frac{1}{C}}{s + \frac{1}{R_f C}}$$

The buffer may or may not be needed in an actual circuit; it is included here merely to preserve polarity in the example.

We will keep this result in mind as it comes to play a frequent role in active circuits. In general then, the impedance when $R \| C$ (read "R is in parallel with C") is:

$$\frac{\frac{1}{C_x}}{s + \frac{1}{R_x C_x}}$$

then it follows that the complete transfer function becomes:

$$\frac{V_o}{V_i} = \frac{\frac{1}{R_i C_f}}{s + \frac{1}{R_f C_f}}$$

Notice that now the break frequency and the gain (as represented by N(s)) are now decoupled and dependent upon two separate circuit parameters: R_i & R_f. Also that when $\omega = 0$, gain has devolved back to an expected $\frac{R_f}{R_i}$, so the plotting equation is:

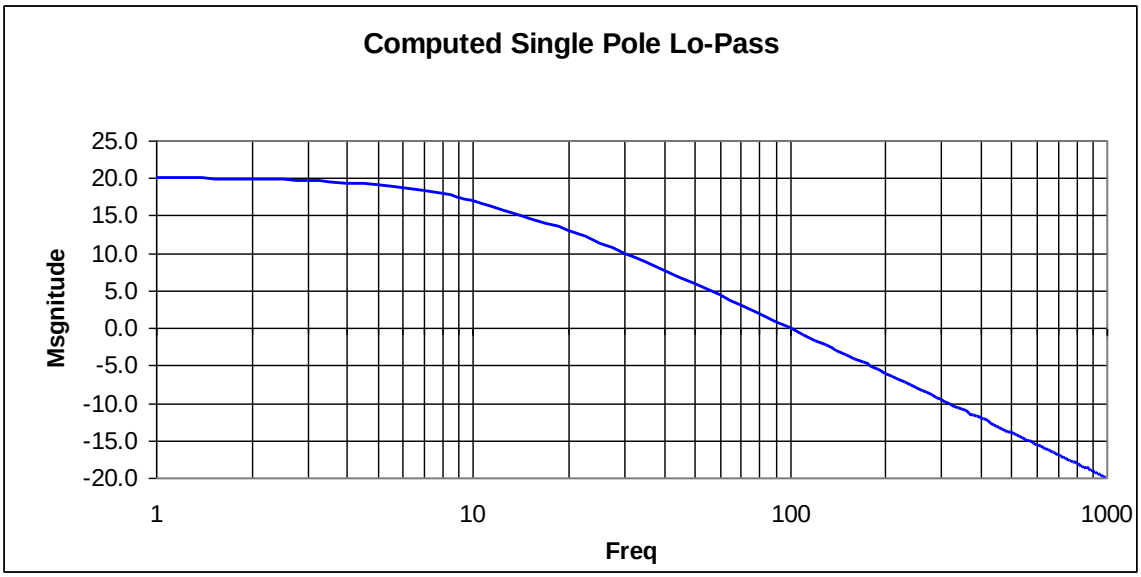
$$Magnitude = 20 \log\left(\frac{R_f}{R_i}\right) - 20 \log\left(\sqrt{1 + \left(\frac{\omega}{\omega_o}\right)^2}\right)$$

where $\omega_o = \frac{1}{R_f C}$. And, of course:

$$Phase = 0 - \tan^{-1}\left(\frac{\omega}{\omega_o}\right)$$

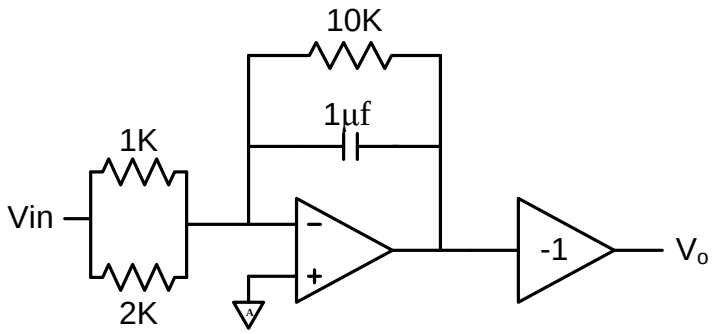
Assuming $R_f C = .1$, and that $\frac{R_f}{R_i} = 10$, then:

$$Magnitude = 20 \log(10) - 20 \log\left(\sqrt{1 + \frac{\omega^2}{100}}\right)$$



The above has the exact same response of the previous lo-pass with a gain of 10 circuit, but with fewer components. Fewer components equal higher reliability and longer MTBF[3], resulting in a more compact circuit. While this case is trivial, it serves to open the door to the design philosophy of component count minimization.

As an exercise, assume that a gain of 15 is needed and the circuit is to have a break frequency at 100 rads/s. Further assume that a 1μf capacitor is chosen. Then since ω_o=100, the time constant is .01; further as C=1X10^{-6}, R_f must equal 10KΩ. Gain is 15 which clamps R_i to 667Ω - a non-standard value.



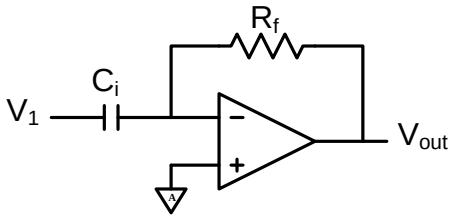
At this point the designer has the option of accepting a non-standard value for R_i or to find some standard component mix of values for capacitance and resistance that will simultaneously satisfy R_fC_f=.01 and R_f=15*R_i - it all depends upon what is acceptable for the production line. A 2KΩ resistor in parallel with a 1KΩ would do the job; but it adds to the component count. A standard value of 680Ω could be used, but the gain will not equal 15. There seems to be no optimum solution; just choices that offer different problematic aspects. Question: How could a change of requirement to a -40db/dec roll-

[3] Mean Time Between Failures

off be handled? Again, in the above circuit, the buffer is included only to preserve polarity in the example; in practice it may or may not be needed.

A Mythical Differentiator

This circuit deserves some serious discussion concerning the convenience of schematic representation versus the realities of the component needs. The conventional schematic is:



First let's consider the transfer function:

$$\frac{V_{out}}{V_{in}} = \frac{-R_f}{\frac{1}{sC_i}} = -sR_fC_i$$

or, re-written:

$$V_{out} = \left(-R_fC_i\right)\left(sV_{in}\right)$$

or, more compactly:

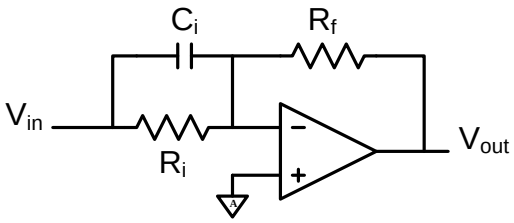
$$V_{out} = K_1 sV_{in}$$

Which says V_{out} equals the derivative of V_{in} scaled by the factor R_fC_i. Clearly this is a very useful circuit. We now have a method of obtaining the derivative of an input, and we retain control over the scale factor. Great! Or is it?

Consider the case when the op-amp has been properly offset such that $V^+ - V^- = 0$, then V_{out} also equals zero. The junction of the capacitor and R_f is now a virtual ground. While that point is at a virtual zero volts potential, you cannot draw current into the op-amp negative input from this virtual ground as no DC current can flow through the capacitor. Bear in mind that in a real circuit, although the bias current is trivial, it is still needed (biases the input gate of an FET). A physical ground is needed. As there is no DC path to ground from the V^- input, proper internal bias cannot be obtained, i.e., the circuit **cannot** be depended on to work as intended. See appendix C for one work-around for this problem.

Differentiator and Gain

Consider the circuit below:



The impedance of the input:

$$\frac{\frac{R_i}{sC_i}}{R_i + \frac{1}{sC_i}} = \frac{R_i}{sC_iR_i + 1} = \frac{\frac{1}{C_i}}{s + \frac{1}{R_iC_i}}$$

is the transfer function:

$$\frac{V_{out}}{V_{in}} = R_fC_i\left(s + \frac{1}{R_iC_i}\right)\angle 180$$

leading to:

$$Magnitude \;\; = 20\log\left(\frac{R_f}{R_i}\right) + 20\log\left(\sqrt{1 + \frac{\omega^2}{\omega_o^2}}\right)$$

$$Phase \;\; = 0 - \tan^{-1}\left(\frac{\omega}{\omega_o}\right)$$

The re-arranged form of the transfer function:

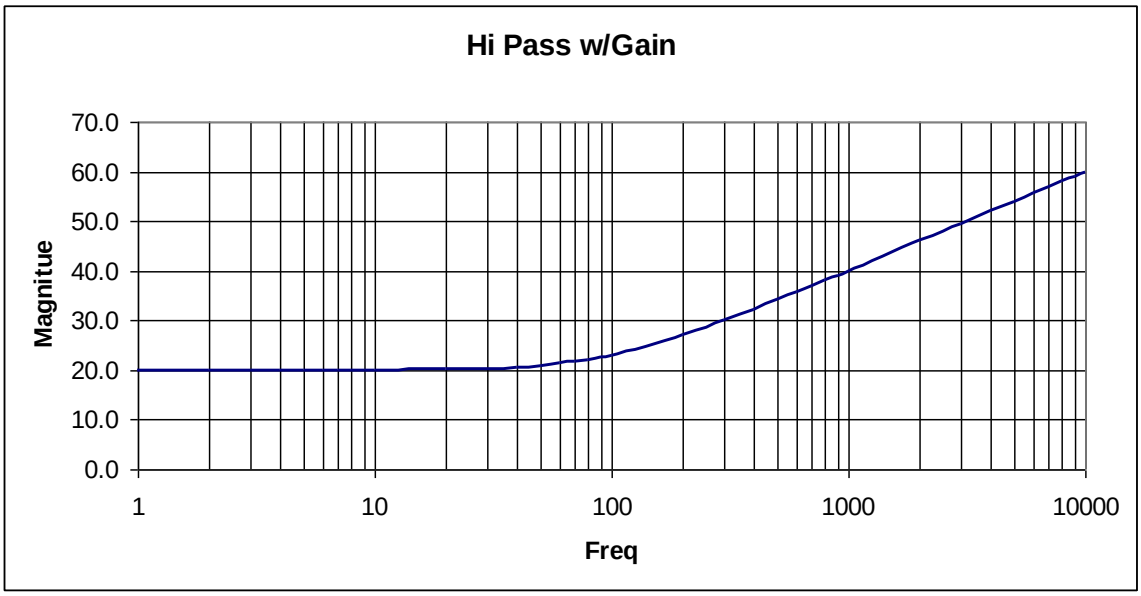
$$\frac{V_{out}}{V_{in}} = -\left(sR_fC_i + \frac{R_f}{R_i}\right) = \left|\left(sR_fC_i + \frac{R_f}{R_i}\right)\right|\angle 180$$

or

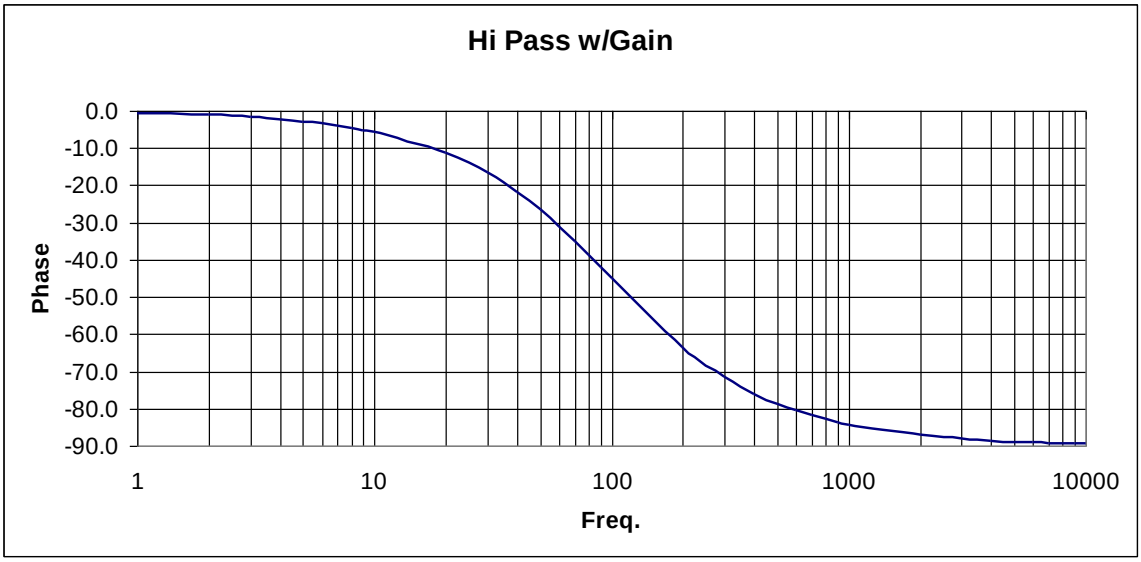
$$V_{out}(s) = K_1sV_{in}(s) + K_2V_{in}(s)$$

is useful in developing a circuit that differentiates. Notice that when s=0, gain is $\left|\frac{R_f}{R_i}\right|$, the common fixed gain inverting amplifier.

For the sake of an example, let ω_o be 100 and a DC (ω=0) gain of 10.



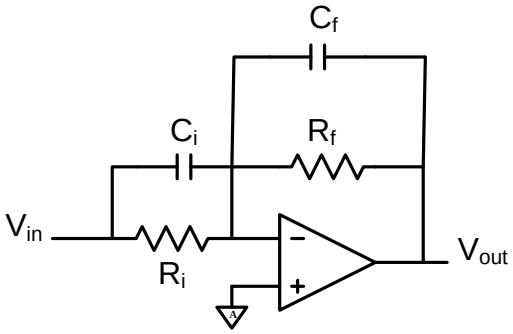
This response is nothing new, but you as the designer have complete control over the gain and break frequency. More importantly as we will shortly see, this circuit, as all the others, is merely a building block. Eventually we will combine these circuits into a transfer function that fits the needs of a design criterion.



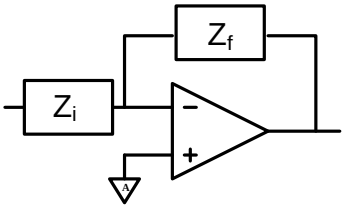
The last circuit we will consider in this module is a combination of the previous circuit and the Integrator/Lo-Pass w/Gain circuit.

Integrator/Lo-Pass w/Gain circuit

The following circuit has interesting and very useful properties. Being a combination of the last two circuits discussed, you might expect that its performance would be a combination of the performances of the previous two. Indeed it is.



For all practical purposes this circuit reduces to:



where:

$$Z_i = \frac{\frac{1}{C_i}}{s + \frac{1}{R_i C_i}}$$

and:

$$Z_f = \frac{\frac{1}{C_f}}{s + \frac{1}{R_f C_f}}$$

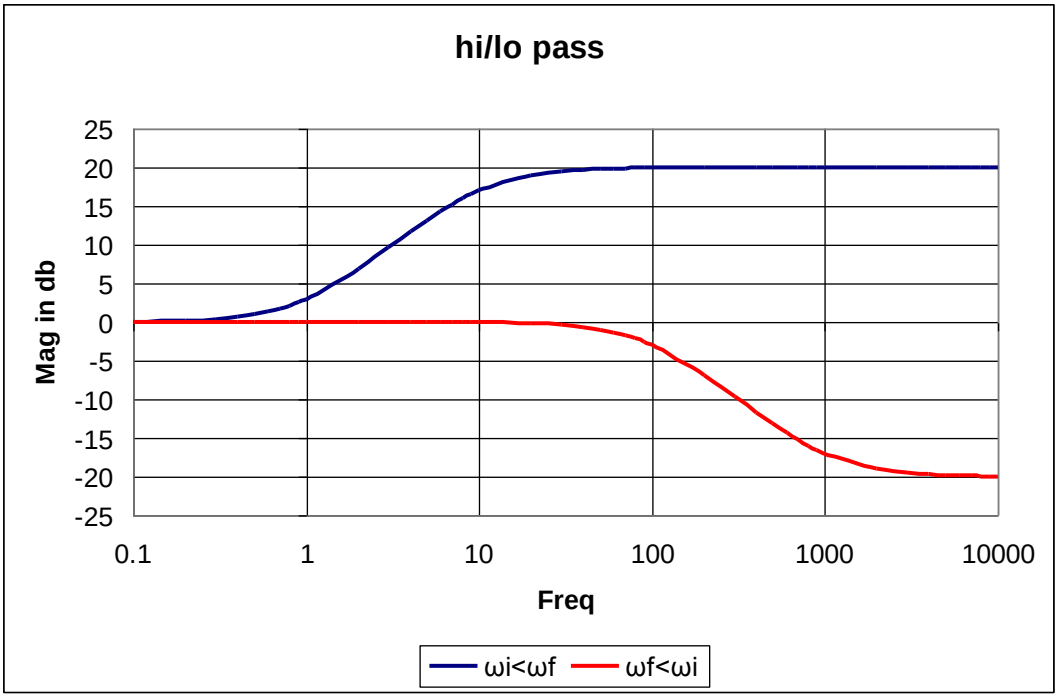
finally:

$$\frac{V_{out}}{V_{in}} = -\left(\frac{C_i}{C_f}\right)\left(\frac{s + \frac{1}{R_i C_i}}{s + \frac{1}{R_f C_f}}\right)$$

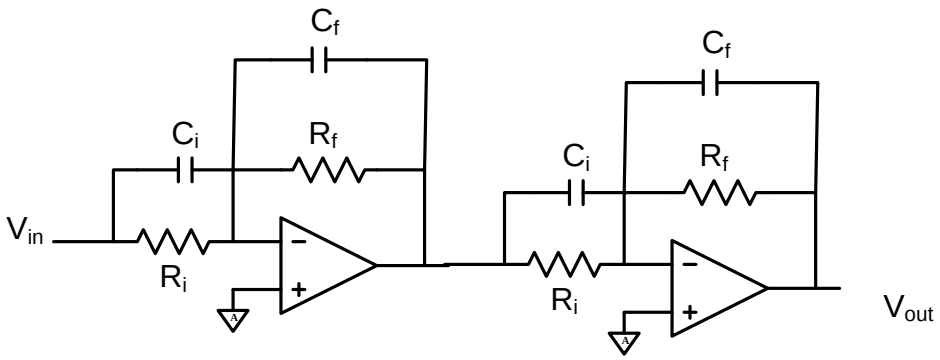
Notice that when $s = 0$ the gain reverts to the expected $-\frac{Rf}{Ri}$, and that when $s >> \frac{1}{R_x C_x}$ the gain $\approx -\frac{sC_i}{sC_f} = -\frac{\frac{1}{sC_f}}{\frac{1}{sC_i}} = -\frac{X_{Cf}}{X_{Ci}}$ also as expected. This yields:

$$Mag. = 20\log\left(\frac{C_i}{C_f}\right) + 20\log\left(\sqrt{1+\left(\frac{\omega}{\omega_i}\right)^2} - 20\log\sqrt{1+\left(\frac{\omega}{\omega_f}\right)^2}\right.$$

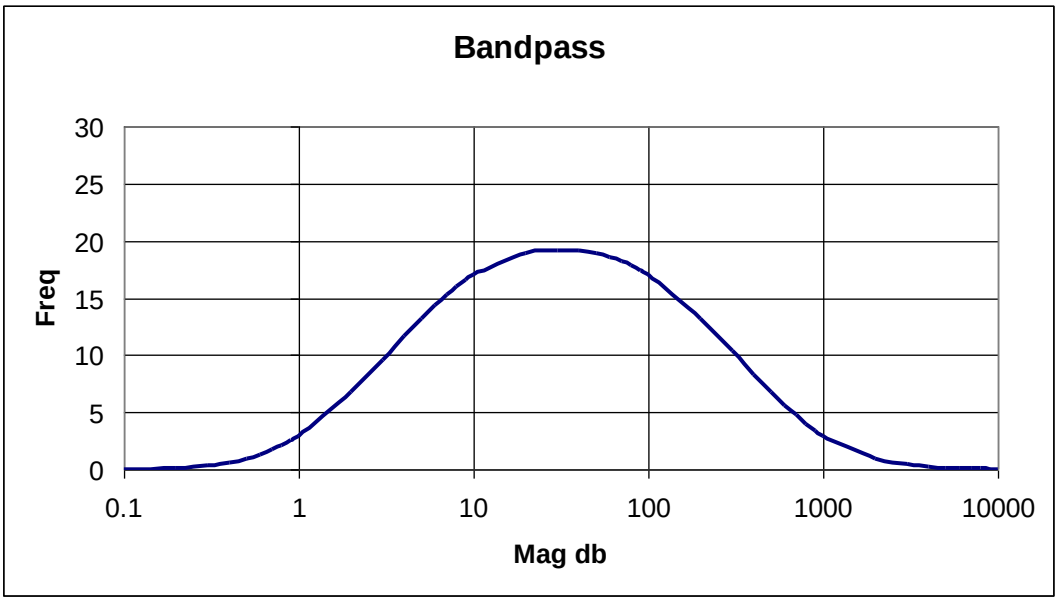
Clearly if $\omega_i < \omega_f$, it is a hi-pass; if $\omega_f < \omega_i$, it is a lo-pass. If we assume that $C_i = C_f$ we have the ability to create either a lo- or a hi-pass by merely choosing resistor values appropriate to the inequalities needed. For example, let the capacitors equal 1μf. If we set the zero break frequency at 1 rad/s then the resistor value is $1x10^6$ Ω. Then if we set the pole break frequency at 10 rads/s, the resistor is $1x10^5$ Ω; we now have a hi-pass. Conversely if we set the pole frequency to 100 rads/s and the zero break frequency to 1000 rads/s with resistor values of $1x10^4$ and $1x10^3$ Ω, we have lo-pass. Notice that the gain is for both plateaus and it does not perpetually increase or decrease.



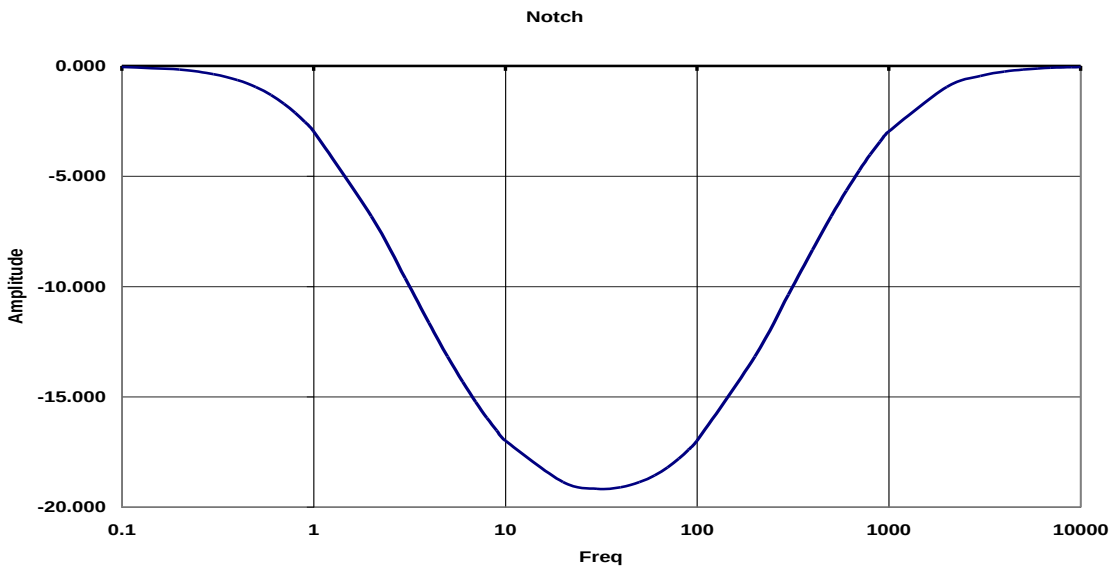
Were we to cascade two of these circuits in series and choosing the zero frequencies to be 1 & 1000 rads/s and the pole frequencies to 10 & 100 rads/s, we get:



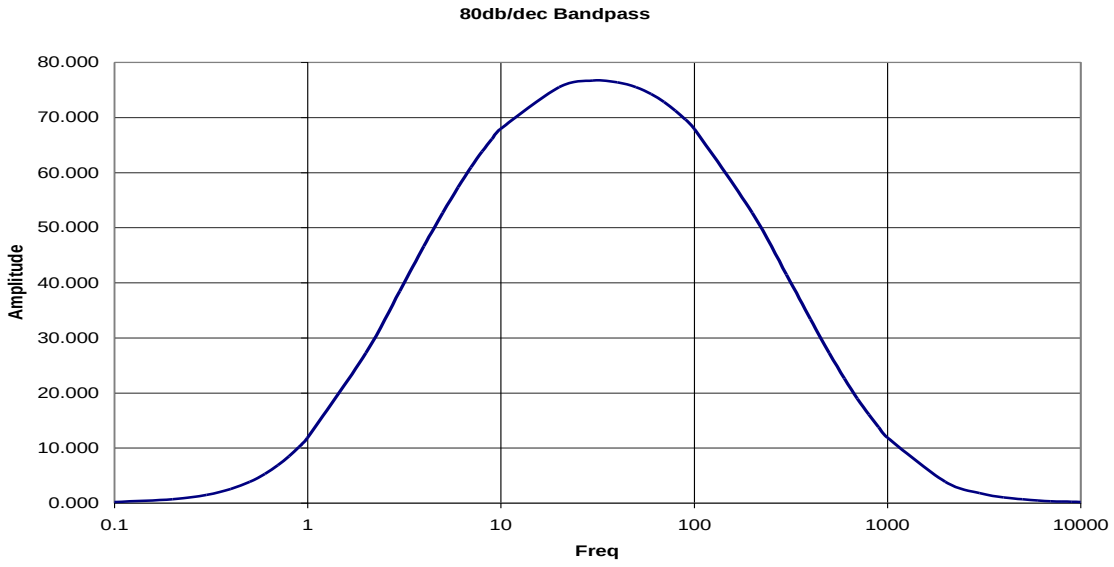
s



Recognize that the slopes and amplitudes can be controlled and adjusted as necessary by cascading additional modules of the same circuit. Footprint on the circuit board is virtually unaffected by cascading when ASIC's are used. Were we to reverse the order of the poles and zeros, i.e., poles at 1 and 1000 rads/s and zeros at 10 and 100 rads/s, we obtain a "notch" filter.



It is for certain that the circuit would have greater utility if the slope were on the order of 80db/dec or greater. In such a case the bandpass filter would look like this:



Notice what happens to bandwidth as the order of the filter is increased from 1 to 4; the bandwidth is decreased by approximately 63%. The salient points are that as the order of the filter is increased, and discrimination and selectivity are enhanced.

The greatest utility is that the circuit whose Bode transfer function is as immediately above, occurs when the base line is moved from 0db to $\approx$-76db. Its utility as a noise

suppression circuit then becomes self-evident. Ponder: What circuit would you use to move the base line to ≈ -76 db (for simplicity use -80db)?

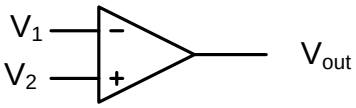
Other circuits will be developed as needed in subsequent modules as needed.

Appendix A

A Look at the Op-Amp Output

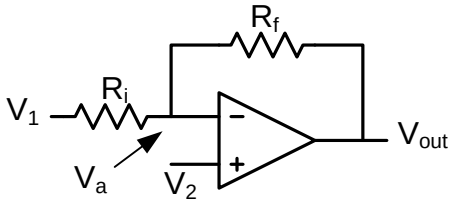
There is a mix of error voltages that occur in practice that are not considered in the elementary general development of op-amp circuit design. These voltages occur in the output independently of the driver. The op-amp is a physical device consisting of transistorized circuitry embedded in a substrate (a "chip") and is often implemented using field effect transistors as the device of choice (in the slide rule days we used vacuum tube triodes). There are solid considerations for choosing FET's, one of which is that the input impedance is extremely high, and bias currents are miniscule. Nevertheless, there are bias considerations that are inescapable in using the physical device.

As a rule, a DC path to ground must be provided for each input, even if it is a sneak path such as the output stage of the driver. Bizarre effects will occur without those paths, often rendering the device unresponsive or unpredictable. That being the case, the assumption made during development that no current flows into the op-amp inputs is not precisely correct. There is a current, often it is in the range of 10^{-6} of that of the external circuit current. So while being imprecise, we can usually ignore the input current. But precision requires that the designer be aware of it and its effects on the gross output.



The input stage of the op-amp produces an output that is proportional to V_2-V_1. That stage is followed by conditioning and amplifying stages such that $V_{out}=K_1(V_2-V_1)$, where K_1 is the value of the open loop gain; a constant on the order of 10^5 or greater. The expression $V_{out}=K_1(V_2-V_1)$ represents the output voltage due to the open loop gain of the op-amp - it will be clamped to a rail.

Consider the following:



where V_2 is at some small potential removed from actual circuit ground caused by bias current, i.e. $V_2 \neq 0$. By extension then $V_a = V_2$. If the circuit is linear (and it better be if it is to be useful as other than a binary device), then:

$$\frac{V_1 - V_a}{R_i} = \frac{V_a - V_{out}}{R_f}$$

doing some re-arranging:

$$\frac{R_f}{R_i}V_1 - V_a\left(1 + \frac{R_f}{R_i}\right) = -V_{out}$$

To differentiate between the various values of $V_{out,}$ assign V_{o1} to the open-loop gain and V_{out} to the closed loop gain. So:

$$V_{o1}=K_1(V_2-V_1)=K_1V_a$$

where K_1 is an intrinsically high value on the order of 10^5 or greater.

$$V_a = \frac{V_{01}}{K_1}$$

Let $\frac{R_f}{R_i} = K_2$, then:

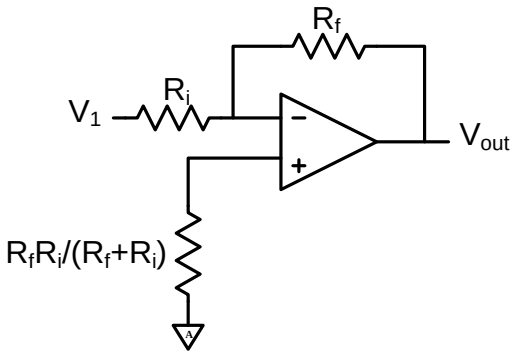
$$K_2V_1 - \left(\frac{V_{ol}}{K_1}\right)(1 + K_2) = -V_{out}$$

Assume $\frac{K_2}{K_1} \approx 10^{-3}$ since K_2 is of the order of 10^2 or less and K_1 is of the order 10^5 or greater. Then:

$$\frac{K_2 + 1}{K_1} \approx \frac{K_2}{K_1} \leq .001$$

$$K_2V_1 - .001V_{ol} = -V_{out}$$

V_{01} can be forced to closely approach 0 in a couple of ways. One is to supply the op-amp's offset input (if it has one) a voltage sufficient to null out V_{01}. Another is to use a bias resistor at the positive input equal to the parallel combination of R_f and R_i.



In the absence of the driver, the bias currents to each input are then the same (or nearly so).

When V_{01} is forced to be 0 then by $V_{o1}=K_1V_a$, V_a must be zero because K_1 is not, leaving:

$$-\frac{R_f}{R_i}=\frac{V_{out}}{V_1}$$

From the defining schematic above, the magnitude of V_2 (the voltage appearing at the junction of R_i & R_f) is:

$$V_2=\left(i^+\right)\left(\frac{R_iR_f}{R_i+R_f}\right)$$

where i^+ is the input current to the non-inverting input. That current is the bias current into the gate of an FET; generally in the nano amp range which puts V_2 about in the 10^{-4} volt range. So FAPP[4] comes galloping to our salvation again (assumes that V_2 is trivial or nearly 0 for practical purposes) wherein the model assumes a zero volt potential at the positive input; allowing the claim that:

$$-\frac{R_f}{R_i}\approx\frac{V_{out}}{V_1}$$

In any event, the expression:

$$\frac{V_o}{V_{in}}=-\frac{R_f}{R_i}$$

is a close approximation of the actual gain, and as a working relationship, is sufficient for almost all uses. But as in the Quantum world, there are little "ghosties" hanging around that the designer must be aware of and account for when precision is necessary.

[4] For All Practical Purposes

Appendix B

Gain Bandwidth Product

The op-amp has internal poles that determine its response as a function of gain and frequency. Fortunately, the response is linear or nearly so, and follows an algebraic relationship.

As a rule, the open loop gain of an op-amp is very high; on the order of 10^5 or greater. However there is a dominate low frequency pole at a very low value; between 2 and 30Hz. From that point, the response linearly falls off in a way such that:

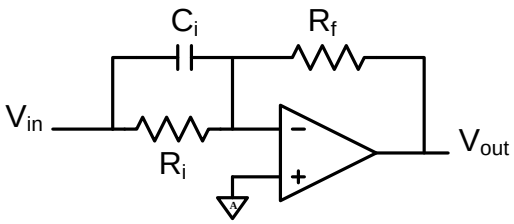
gain*bandwidth=constant.

For example if the device has a bandwidth of 10^6 at a gain of 1, it will have a bandwidth of 10^5 at a gain of 10, a bandwidth of 10^4 at a gain of 100, and so on. This device would be identified as having a GBW (gain bandwidth product) of 10^6 (GBW being defined at a gain of 1).

Appendix C

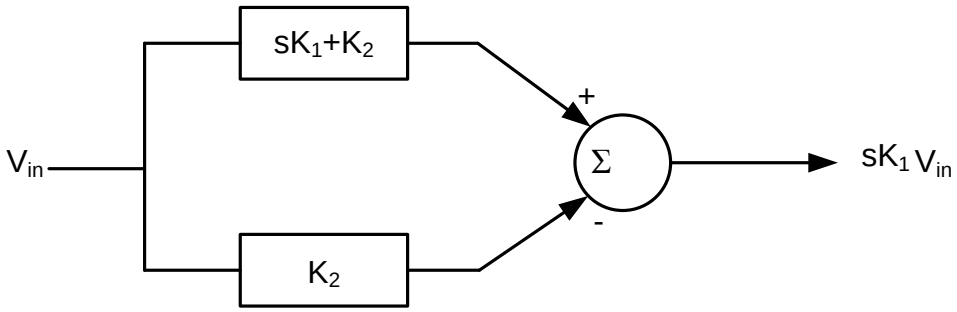
Differentiator

Recall that this circuit has a transfer function of:



$$\frac{V_{out}}{V_{in}} = sR_f C_i + \frac{R_f}{R_i}$$

Using block diagrams, this transfer function suggests to yield a differentiator:



While the component count exceeds that of the circuit consisting of an op-amp, a resistor and a capacitor, its dependability to avoid the issue of an ungrounded (DC wise) input is assured. Therefore its ability to deliver a dependable output is assured.

Appendix D

Table of Transforms

Transform	$f(t)$	$F(s)$
1	K	$\frac{K}{s}$
2	$Ke^{-\sigma t}$	$\frac{K}{s+\sigma}$
3	$K\sin(\omega t)$	$\frac{K\omega}{s^2+\omega^2}$
4	$K\cos(\omega t)$	$\frac{Ks}{s^2+\omega^2}$
5	$Ke^{-\sigma t}\sin(\omega t)$	$\frac{K\omega}{(s+\sigma)^2+\omega^2}$
6	$Ke^{-\sigma t}\cos(\omega t)$	$\frac{K(s+\sigma)}{((s+\sigma)^2+\omega^2)}$
7	$\delta(t)$	1
7a*	$K\delta(t)$	K
8	$Ku(t-a)$	$\frac{Ke^{-as}}{s}$
9	$f'(t)$	$sF(s)-f(0)$
10	$\int f(t)dt$	$\frac{F(s)}{s}+\frac{f(0)}{s}$
11	$af(t)+bg(t)$	$aF(s)+bG(s)$
12	t	$\frac{1}{s^2}$
13	te^{-at}	$\frac{1}{(s+a)^2}$

Table 1

(*) K is preserved for practical circuit reasons, not for theoretical reasons as $K * \infty$ *is approximately equal to* ∞.

Table 1 is not all inclusive and other pairs will be examined and added when needed. But for beginning analysis purposes, Table 1 is adequate.

It is very important to understand that to be able to transform any $F(s)$ to an $f(t)$, $F(s)$ must be reduced to one of the forms so far developed. If it is not in one of these forms, for the purposes of this course it cannot be operated on until it is. Study the right hand side forms as they identify the left hand side.

Transforms 12 and 13 are found as follows:

$$f(t) = t$$

$$F(s) = \int_0^\infty te^{-st}dt = \frac{1}{s^2}$$

For transform 13, assume:

$$f(t) = te^{-at}$$

$$F(s) = \int_0^\infty te^{-(s+a)t}dt = \frac{1}{(s+a)^2}$$

Finding transforms 12 and 13 is a straight forward exercise using integration by parts.

Appendix E

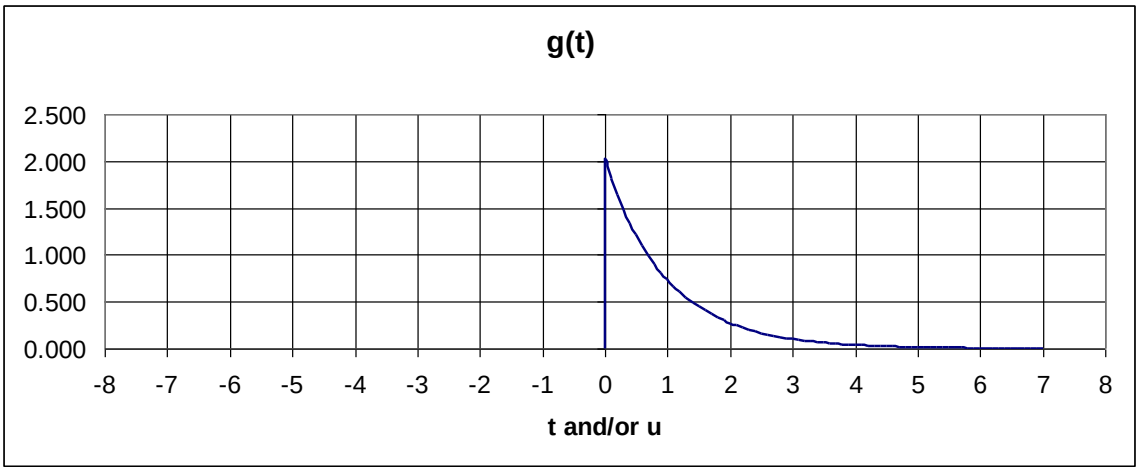
Convolution and LaPlace Domain Multiplication

Consider the following integral:

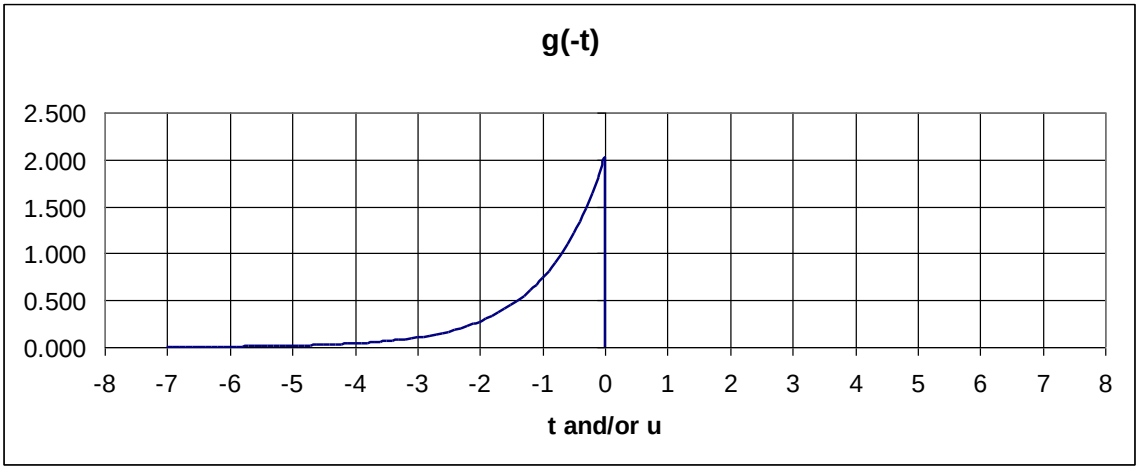
$$h(t) = \int_0^t f(u)\,g(t-u)\,du$$

For the sake of illustration, read the above integral this way: let $f(u)$ be a transfer function in the time domain, and $g(t-u)$ be a signal.

Begin by building the signal this way, $g(t) = e^{-t}$.

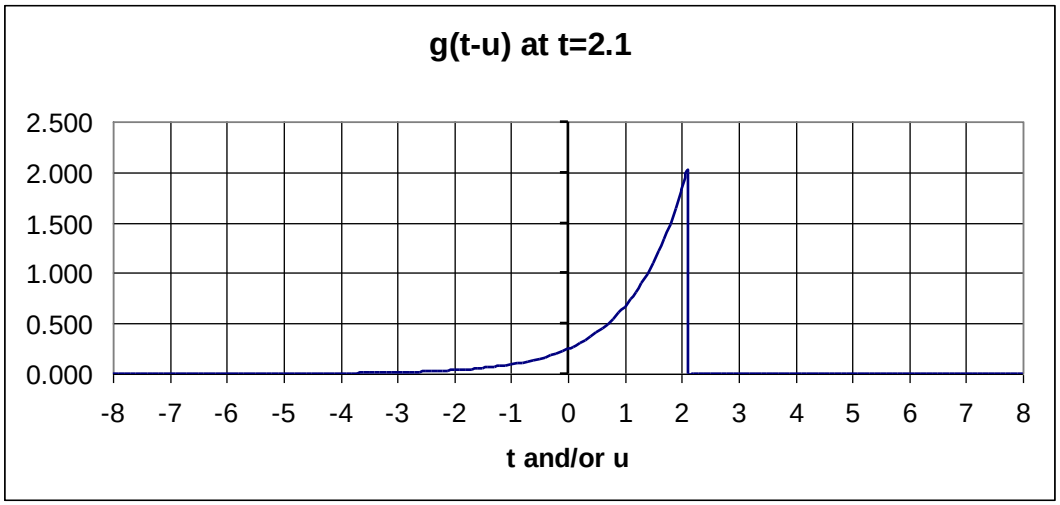


Now "flip" the signal horizontally, so that as it progresses left-to-right, the leading edge is *g(0)*.



Now let *g(-t)* proceed left to right. Recognize that "*u*" is a dummy variable of integration and that physically $u = t$ for every *u* and *t*. Therefore *g(t-u)* always equals *g(0)* regardless of where it is on the *x* axis.

Arbitrarily assume the limit on the integration is 8. At $u = t = 2.1$, *g(t-u)* would be:



At *t*=2.1, *g(t-u)=g(*2.1-2.1*)=g(0)*; but when *t*=2.1 what does *g(t-*1*)* look like? Well *g((*2.1-1)-2.1*)=g(*-1.1*)*. And if you check the value of *g*(-1.1) on the graph of *g(-t)*, you will see that they agree with the value on the graph on the previous page at t=-1.

Therefore the argument *(t-u)* is interpreted to mean that the signal is flipped 180^o horizontally, allowing *g*(0) to be the leading edge of the signal passing through the transfer function. This is the **convolution integral** and it expresses mathematically the physical property that a signal passes through a transfer function as the right-to-left mirror image of that seen on an oscilloscope. Note that it is irrelevant whether we consider the signal passing through the transfer function or the transfer function passing through the signal; our view has no effect on the outcome.

That being the agreed case, the following pair is defined:

$$\int_0^\infty h(t)e^{-st}dt = f(s)g(s)$$

where:

$$h(t) = f(t)g(t-u)$$

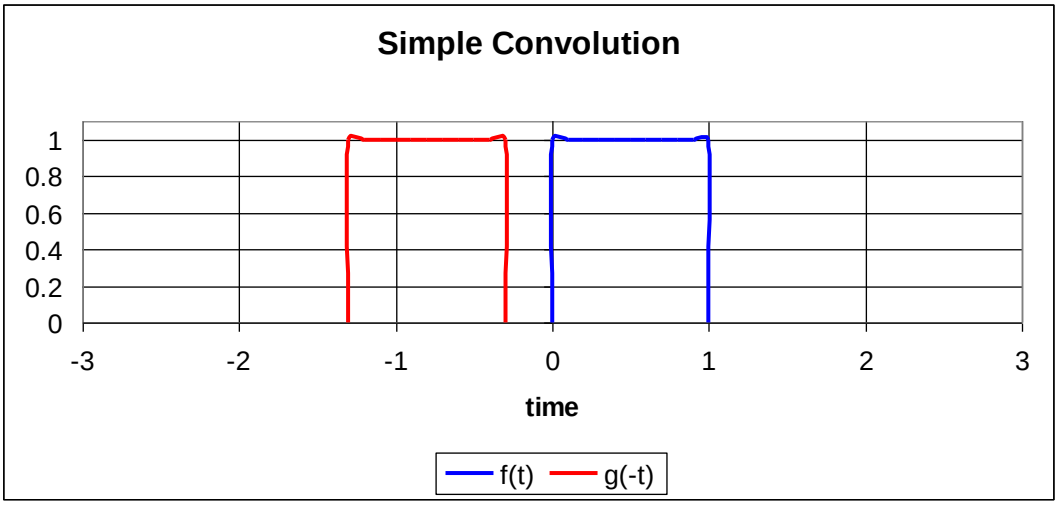
tying the physical property of passing a signal through some hardware to the LaPlace transform of that process.

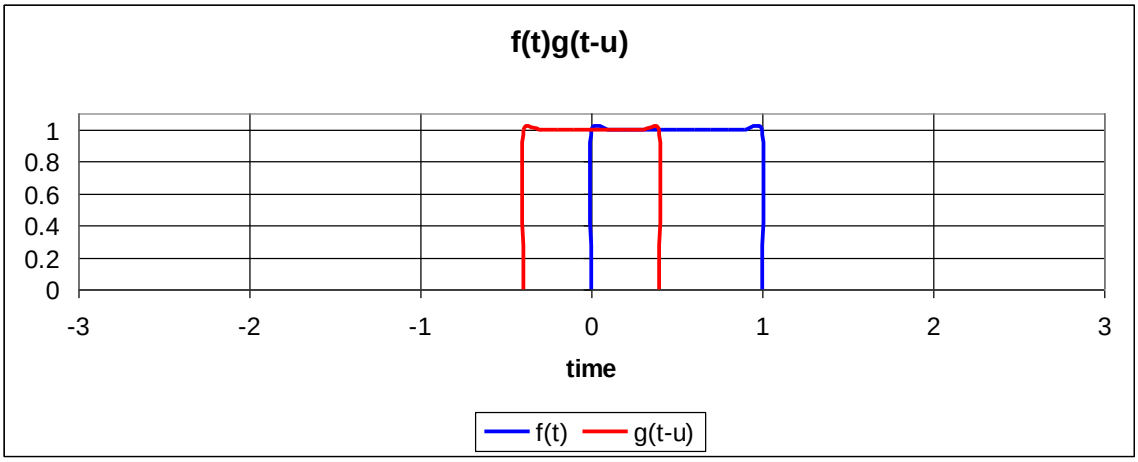
Suppose $f(t) = u(t) - u(t-1)$ and that $g(t) = u(t) - u(t-1)$, then the transform would be:

$$f(s)g(s) = \frac{1}{s}\left(1 - e^{-s}\right) * \frac{1}{s}\left(1 - e^{-s}\right) = \frac{1}{s^2}\left(1 - 2e^{-s} + e^{-2s}\right)$$

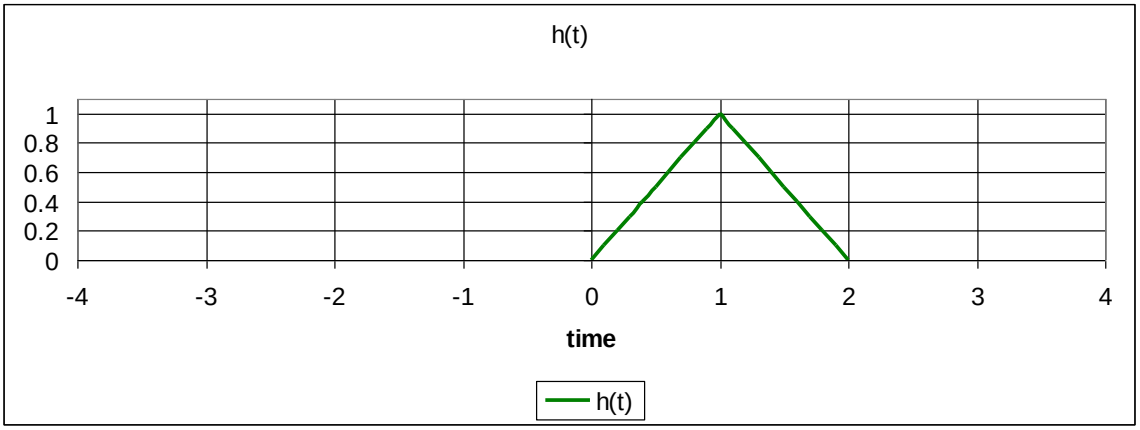
The time result would be:

$$h(t) = t * \left(u(t) - 2u(t-1) + u(t-2)\right)$$





h(t) is the integral of the area where *f(t)* intersects *g(t-u)*. After *g(t-u)* completely passes through *f(t)*, the results of the integral are:



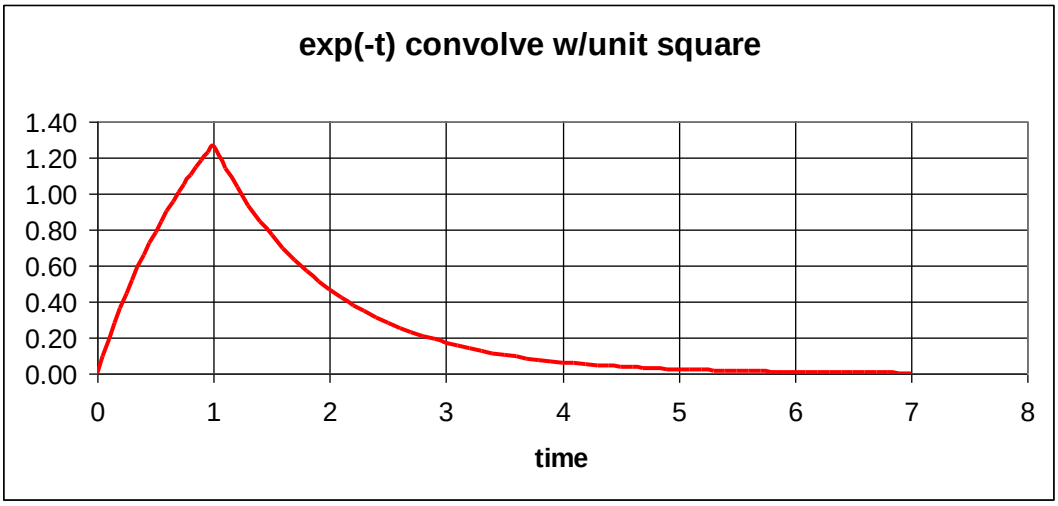
This result agrees with the results of the time domain inversion of *f(s)g(s)*. You may verify that this result is indeed the solution in the time domain by visiting http://jhu.edu/signals/convolve/index.html; courtesy of Johns Hopkins University, or by obtaining *h(t)* on the interval 0-2 using the convolution integral.

Reverting to $g(t) = 2e^{-t}$ and using $f(t) = u(t) - u(t-1)$; then in the Laplace domain:

$$f(s)g(s) = \left(\frac{1}{s} - \frac{e^{-s}}{s}\right)\left(\frac{2}{s+1}\right) = \left(\frac{2}{s(s+1)}\right)\left(1 - e^{-s}\right)$$

Taking the inverse transform and plotting:

$$h(t) = 2(1 - e^{-t})u(t) - 2(1 - e^{-t})u(t-1)$$



Again, you may verify that this result is indeed the solution in the time domain by visiting http://jhu.edu/signals/convolve/index.html; courtesy of Johns Hopkins University, or by obtaining *h(t)* using the convolution integral.